AMENDMENTS TO THE CLAIMS

In accordance with the revised format for making amendments as set forth in 37 C.F.R. § 1.121, amendments to the claims are made with additions being indicated by way of underlining and deletions being indicated by way of strikethroughs. Further, each claim is provided a status identifier in parenthetical immediately preceding each respective claim and indicating whether or not it is an original, previously presented, presently amended, or new claim.

1-11. (Cancelled)

12. (Allowed) A process for making an interconnect for attaching a multi-chip module to a circuit substrate comprising:

providing a member elongated in a longitudinal direction;

forming a series of circuit pads on opposing major faces of said member, said circuit pads being arranged in at least two lines in said longitudinal direction on each of said major faces, with the circuit pads in a line on one side of said member being aligned with respective opposing circuit pads on the other major face of said member;

forming a series of openings in said circuit pads extending through said member and at least one circuit pad on one of said major faces and at least another circuit paid on said opposing major face, said openings being arranged ins aid at least two lines;

forming a conductive metallization in said openings electrically connecting each of said one circuit pads to a respective one of said another circuit pads;

dividing said member along a generally central axis of said openings in said at least two lines to provide at least one interconnect member having at least a first elongated side and a second opposed and generally parallel elongated side, said first and second sides extending in said longitudinal direction;

each of said first and second sides having at least one castellated portion formed by a series of metallized depressions in said respective first and second sides extending inwardly from a first outer surface of said first side and a second outer surface of said second side; and

wherein said depressions form castellated leads.

13. (Allowed) The process as in claim 12 wherein the step of forming said openings comprises drilling holes through said member and centrally of opposing circuit pads on the opposing faces of the member, whereby said depressions have a generally semi-cylindrical shape.

14. (Allowed) The process as in claim 13 wherein each of said first and second sides extends from a first transverse end of said interconnect member to a second transverse end of said interconnect member; and wherein a portion of each of said sides, intermediate said ends is formed without castellated leads.

15. (Allowed) The process as in claim 3 wherein said member is provided with third and fourth opposed elongated sides extending respectively between said first and second sides and

wherein the portion of each of the third and fourth sides associated with the non-castellated portions of the first and second sides is formed for receiving a pick and place assembly device.

16. (Presently Amended) A process for attaching a multi-chip module to a circuit substrate comprising:

providing a multi-chip module having a plurality of electronic elements;

providing a circuit substrate supporting thereon a conductive circuit pattern adapted for connection to said multi-chip module;

providing at least one interconnect member for attaching said multi-chip module to said circuit pattern on said circuit substrate, said interconnect member comprising:

a member elongated in a longitudinal direction, said member having at least a first elongated side and a second opposed and generally parallel elongated side, said first and second sides extending in said longitudinal direction;

each of said first and second sides having at least one castellated portion formed by a series of depressions in said respective first and second sides extending inwardly from a first outer surface of said first side and a second outer surface of said second side;

wherein said interconnect member is formed by generating a series of circuit pads on opposing major faces of said member arranged in at least two lines in said longitudinal direction on each of said major faces, forming a series of openings in said circuit pads extending through said member and at least one circuit pad on one of said major faces and at least another circuit pad on

said opposing major face; and dividing said member along a generally central axis of said openings to provide at least one interconnect member;

wherein said depressions are metallized to form castellated leads for connecting at least one electronic element of said multi-chip module to said conductive circuit pattern of said circuit substrate;

forming a sub-assembly by attaching said at least one interconnect member to said multi-chip module to make a desired electrical connection between at least one of said castellated leads of said interconnect member and said at least one electronic element; and

attaching the sub-assembly to the circuit substrate to make at least one desired electrical connection between said at least one castellated lead of said interconnect member and said conductive circuit pattern of said circuit substrate.

17. (Original) The process as in claim 16 further comprising having each of said first and second sides of said interconnect member extend from a first transverse end of said member to a second transverse end of said member; and forming in each of said sides at least one portion, intermediate said ends which is not castellated.

18. (Original) The process as in claim 17 further comprising providing said interconnect member with third and fourth opposed elongated sides extending respectively between said first and second sides and wherein the portion of each of the third and fourth sides associated with the non-

castellated portions of the first and second sides is formed to receive a pick and place assembly device.

19. (Original) The process as in claim 18 wherein a plurality of said interconnect members are attached to said multi-chip module and said circuit substrate.

20. (Original) The process as in claim 19 wherein said multi-chip module includes a first major face and a second opposed major face and wherein first electronic elements are provided on said first face and additional second electronic elements are provided on said second face and employing said interconnect members to space said multi-chip module from said circuit substrate by an amount greater than the thickness of electronic elements arranged on said multi-chip module between said multi-chip module and said circuit substrate.

21. (Original) The process as in claim 20 further comprising providing at least two of said interconnect members to connect said multi-chip module to said circuit substrate and attaching each of said interconnect members toward a different edge of said multi-chip module.

In making the above amendments, no new matter is believed added.